A. CV and personal information:

Dr. Michael F. Dossis (EngDip, PhD)
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1. Design, development and research activities at Intracom

During his employment by Intracom Dr Michael F. Dossis has offered the following engineering services and/or achieved and contributed to the company the following:

1. Successful organizing, coordination, assembling, composition and submission of research proposal for funding by the European Community (Adriatic).

2. Successful modeling, coding in VHDL and development without functional errors of the 4 WIBAS convergence layer IP blocks (2 BS + 2 SS).

3. Investigation, and development of the first functional testbenches for the WIBAS project, and integration into these testbenches of all the VHDL code for FPGAs that had been developed for this project.

4. Production of executable specifications in VHDL code of excellent quality regarding the code's readability and absence of any serious functional errors.

5. Successful investigation and development of the first VHDL models for the clock generators suitable for implementation in Xilinx FPGAs (DCMs). Successful integration and use of these Xilinx DCM models as well as of their functional equivalent models which were developed from scratch by Dr Dossis.

6. Successful investigation and development of the new bottom-up design flow (using Leonardo & Xilinx ISE), which was used for integration and implementation of all the WIBAS project VHDL blocks. The FPGA implementations produced using this flow, operated first-time right in the laboratory prototypes, without any problems due to the developed design flow. This work included the integration and use of all the involved tools as well as the setup and execution scripts to run these tools in the bottom-up design flow.

7. Successful investigation and development of the new top-down design flow (using Synplify & Xilinx ISE), which was used for integration and implementation of all the WIBAS project VHDL blocks with the new tool Synplicity Synplify. The FPGA implementations produced using this flow, operated first-time right in the laboratory prototypes, without any problems due to the developed design flow. This work included the integration and use of all the involved tools as well as the setup and execution scripts to run these tools in the bottom-up design flow.

8. Successful investigation, development and execution of all the command files (scripts) on the synthesis tools Synplicity Amplify-RC, Static Timing Analysis tools (Synopsys PrimeTime) as well as integration of all the WIBAS ASIC VHDL code (2.6 Million gates) in the LSI Logic design flow. He was the lead engineer, had the responsibility of, coordinated and monitored the project WIBAS ASIC using software aids such as the Microsoft Project Planning tools.

2. Industrial R&D and Academic/research experience:

2000-2007: **Senior electronics (VLSI) design engineer** in a telecom product design company (Microelectronics Lab, Broadband Systems Department, Intracom S.A., Athens). Organising, assembling and submission of large European Research Proposals (Adriatic). Design of customised digital hardware using VHDL and targeting of designs onto large FGPAs and on large ASICs using LSI-Logic RapidChip ASIC flow. Application area is broadband wireless telecommunications.

15/7-30/9/99: **Senior VLSI design engineer** in a telecom/network processor product company (Virata Ltd, now Connexant, Cambridge, England, UK). Evaluation of tests for existing processor IC and working with marketing for the definition of new communication (TDM) IC products.

1998-1999: **Senior VLSI design engineer** in embedded microprocessor - based products, System-on-chip group (ARM Ltd -UK). Multimedia interfaces (specification, RTL design+synthesis, integration, validation, product reviewing), upgrading of IP blocks (RTL, synthesis, testbenches and functional verification, scan insertion & ATPG, timing annotation) and processor core synthesis and test.

1997-1998: **Senior VLSI product engineer** in Set Top Box Group, LSI Logic Europe. Design of the next generation MP@ML, MP@HL integrated video decoders (microarchitecture specification, design flow, implementation, integration, RTL/testbench design and test).

1996-1997: **Senior VLSI coreware engineer** in custom microprocessors implemented as hard-macro VLSI cores, DSP CoreWare Group, LSI Logic Europe. Design, application support, documentation and verification; RTL coding, testbench design, mixed VHDL+Verilog simulation, proprietary design and re-targeting tools, test generation, embedded software & applications.

1990-1991: **Technical Manager**, microprocessor-controlled hybrid mechanical and hydraulic robotic systems used in automated biochemical analysis machines. Dep. of automated bio-analysis, Medicon Hellas S.A., Athens. Programming, configuration, calibration, promotion, sales, and overall responsibility for customer support.

3. Academic qualifications, research and teaching experience:

1984-1990: ***Higher Diploma in Electronic and Electrical Engineering***, National Technical University of Athens with the following options:
- Graduation project: Digital Communication Systems: "custom ASIC design for high-speed telecommunications" (using ES2 ASIC tools). Supervising academic: Prof E. Protonotarios
- Electronics and telecommunications; digital, analog and electronic system design; digital communications, networks, digital signal processing.
- Digital design, VLSI/ASIC design.
- Microprocessors and computer architecture.
- Automated & microprocessor driven control.
- Computer languages/architectures, software engineering, data structures and data bases.
- Personal interest and training in Logic Programming with Prolog, databases and expert systems

1991-1994: ***PhD in Electronic and Electrical Engineering***, University of Bradford, UK. Title: "Applicability of Programming Code to Hardware Specification and Synthesis".
Theoretical and practical knowledge gained in:
- ASIC/FPGA design using E-CAD tools; CADENCE, ABEL, EPLD, Xilinx and Altera design
- Computer modelling languages, compiler technology, Hardware Description Languages (VHDL, Verilog); high-level synthesis, hardware-software co-design, electronic CAD technology, chip design methodologies, logic

programming and provably-correct hardware compilation using Prolog
- Advanced microprocessor & computer architectures (parallel and pipeline design, DSP, communications); microarchitecture (FSM, data-path & I/O) design
- Real-time and embedded system design (Ada and Motorola 68000)
- Hardware algorithms for encryption, data coding, public-key cryptography
- Teaching, lab supervision, training course planning, presentations or work & training material; project planning, proposals for research funding

1994-1995: ***PACE Teaching Company Scheme***, University of Bradford.
Activities:
- Responsible for designing the syllabus and module/tutorial structure, and lecturing of new final year BSc/MSc modules (DSP processor architectures, ASIC design).
- Training material preparation and management (Industrial Diploma).
- Involved in design of the industrial placement module, training handbooks, assessment methods.

1995-1996: ***Post-doctoral Research Officer***, (the) University of Oxford, Computing Laboratory:
- Rapid prototyping and hardware compilation of parallel (Occam) programs using transputers and Xilinx 3000, 4000 & 6000 FPGAs.
- Hardware/software codesign using parallel processors and high density FPGAs.
- Designed and developed the back-end translator (EDIF) for the Handel hardware compiler.
- Computer languages and formal design methods.
- Parallel design and Handel (an Occam-based parallel modelling language).
- Meta-programming with the Standard New Jersey Meta-Language
- HTML and WEB programming
- Presentation of research work, papers, and technical authoring.
- GNU standard tools (EMACS, etc.) and UNIX-based development
- 3rd year engineering module lab teaching (semi-custom ASIC design)

2007-Oct. 2012: **Assistant Professor** in the department of Informatics and Computer Technology, Technological Educational Institute of Western Macedonia, Kastoria, Greece. Teaching the modules: Structured and Object-oriented programming, Computer Architecture, Advanced (parallel) Architectures, Combinational and Sequential Digital Circuits, Structural (ANSI-C) and Object-Oriented (C++) programming.

Nov. 2012-June 2017: **Associate Professor** in the department of Informatics and Computer Technology, Technological Educational Institute of Western Macedonia, Kastoria, Greece. Teaching the modules: Structured and Object-oriented programming, Computer Architecture, Advanced (parallel) Architectures, Combinational and Sequential Digital Circuits, Design of Embedded VLSI Systems, Design of Digital Systems with VHDL.

July 2017-today: **Professor** in the department of Informatics Engineering, Technological Educational Institute of Western Macedonia, Kastoria, Greece. Teaching the modules: Structured and Object-oriented programming, Computer Architecture, Advanced (parallel) Architectures, Combinational and Sequential Digital Circuits, Design of Embedded VLSI Systems, Design of Digital Systems with VHDL.

4. Skills, experience and research interestes

Digital circuit/system modelling and large FPGA & ASIC implementation, special-purpose processor architectures for applications in data-encryption/security/compression, real-time DSP, computer arithmetic for VLSI, broadband communication applications, compilers & software engineering (with imperative, functional, logic and concurrent programming languages). Moreover, I have hands-on industrial experience as technical manager in robotic control systems (robot arms, hydraulic parts, opto-measurement circuits, all microprocessor controlled) for automated bio-chemical analyser systems and computer hardware, and more recently as a senior VLSI coreware design engineer.

My work in VLSI/ASIC design included EDA tools and systems (including Synopsys, Cadence, Solo (ES2), Viewlogic, Mentor Graphics, Xilinx, Altera tools); extensive use of software and hardware modelling languages for specification, modelling, simulation and design implementation (Model, VHDL, Verilog, Abel and Abel-like), standard and proprietary design languages, intermediate/library design database formats (EDIF, Verilog, SDF, NDL), with technologies such as CMOS gate array, standard cell, semi-custom, full-custom, and FPGAs. Worked on electronic circuits and systems at all abstraction levels (algorithmic, behavioural, functional, RTL, logic), design re-targeting, complex chip-system integration and test methodologies and pattern generation.

Microprocessors, computer and custom VLSI architectures (parallel, data-flow, RISC, Harvard); applications in DSP, control, data coding, cryptography, telecoms. Design of hardware to hardware and hardware to software interfaces. Programming experience using imperative, formal, parallel, real time (Ada, Pascal, C, Occam, Fortran, Intel, Matlab), assembly languages (VME with MC68000/TI/Embedded code), logic-declarative (Prolog) and functional programming (ML) languages. General/special-purpose, off-the-shelf and embedded core DSPs, logic/object programming methodologies. WWW and HTML programming and its browsers (NCSA Mosaic, Netscape). Practical experience in operating systems, (DOS/WINDOWS and UNIX) and shell programming, unix-tool programming windows interfaces, etc.

Applied computer science, compiler technology and computer language design and tool implementation (parsers, semantic transformations, high-level optimisations, etc.). Formal specification methods for computer languages and high-level design tools for digital systems. An Ada-based high-level synthesis compiler developed by the applicant, which generates automatically synthesizable RTL models from software programs.

Technical management (theoretical & practical), project planning, customer contact and technical authoring. Microprocessor based control and robotics for biomedicine. Consultancy and industrial design/control. R&D proposals, project planning/execution.

5. Technical areas of expertise and high potential for contribution in the following:

Computer science and computing:
- computer/modelling languages; theory, specification and design
- compiler technology; theory and implementation. OOP based visualisation tools
- computer system design
- logic programming (Prolog), AI, expert systems

Electronic Design Automation & ECAD tools:
- ECAD for VLSI; circuit modelling (in depth VHDL, Verilog, ABEL, Model); High-level synthesis, RTL synthesis, logic synthesis, silicon compilers.
- Simulation & Synthesis tools: Synopsys Design Compiler, Mentor Graphics tools, Modelsim, Cadence Synergy, Synplicity Synplify/Amplify, Leonardo Spectrum, Xilinx ISE, ES2 SOLO
- Timing Designer
- FPGA technologies: XILINX, ALTERA
- Industry standards, Ada, VHDL, Verilog, EDIF; retargeting and design translating tools.
- Hardware/software codesign, real-time design, HDLs, techniques and tools for Electronic Design Automation environments.
- Formal methods in hardware, interface and system design and verification (Lambda tools, Checkoff tools, model compare and equivalence proof). Knowledge of Formal & Mathematical models that support formal tool cores (e.g. predicate / duration calculus, denotational semantics, temporal logic, state-diagrams, FSM transformations, etc.).

ASIC/custom digital design & applications:
- custom architectures for DSP (filtering, FFT, off-the-self & embedded processors), data coding, compression, security (encryption, cryptography) and MPEG
- (tele-)communications (networks, broadband, data coding)

- hardware/system specification, design, modelling and simulation
- embedded, highly optimised cores and VLSI/ULSI design; gate arrays, FPGAs, standard cells (ES2, Mietec, Xilinx and state-of-the-art Xilinx, Altera);
- symmetric and public-key cryptography, signature coding and linear encryption systems.
- video coding and MPEG-2
- broadband telecom architectures and their VLSI implementation (IEEE 802.16)

6. R&D technical reports and publications:

6.1 Industrial R&D technical documents:

1 Internal marketing requirements and engineering requirements document for new communication products (Virata Ltd).

2 Various internal design flow documents, IP block reviews, internal specification document for a complete multimedia communications embedded product port (ARM Ltd).

3 Two internal design specification documents for unified memory addressing units for MP@ML and MP@HL MPEG-2 video decoders (LSI Logic).

6.2 Research publications:

A. International scientific journals with peer-review

1 Michael Dossis, "Intermediate Predicate Format for Design Automation Tools", Journal of Next Generation Information Technology (JNIT), vol. 1, no. 1, pp. 100-117, May 2010.

2 Michael Dossis, "Provably-Correct, Behavioural, High-Level Synthesis of Program Accelerators via the Web", Journal of Next Generation Information Technology (JNIT), vol. 1, no. 1, pp. 47-60, May 2010.

3 Michael Dossis, "Automated Extraction of Hardware Accelerators via an Intelligent Knowledge-based System", International Journal of Intelligent Information Processing (IJIIP), vol. 1, no. 2, pp. 14-31, December 2010.

4 Michael F. Dossis, "A Formal Design Framework to Generate Coprocessors with Implementation Options". International Journal of Research and Reviews in Computer Science (IJRRCS), Vol. 2, No. 4, August 2011, ISSN: 2079-2557, Science Academy Publisher, United Kingdom, www.sciacademypublisher.com, pp. 929-936.

5 Michael F. Dossis, "Formal ESL Synthesis for Control-Intensive Applications," Advances in Software Engineering, Hindawi Publishing Corporation, vol. 2012, Article ID 156907, 30 pages, accepted 14 April 2012. doi:10.1155/2012/156907.

6 Michael F. Dossis, and Dimitris E. Amanatidis, "Image Processing Hardware using Cellular Neural Networks and High-Level Synthesis", Journal of Computer Vision and Image Processing, NewWorldPub Journal, ISSN 2160-3898, vol. 2, no. 4, December 2012, pp. 29-37.

7 Michael F. Dossis, and Dimitrios E. Amanatidis, “Synthesizing Neural Nets into Image Processing Hardware”, Journal of Pattern Recognition and Intelligent Systems (PRIS), vol. 1, iss (no.) 1, May 2013, pp. 10-17.

8 Michael Dossis, “Rapid Modelling and Verification in the Intelligent CCC Synthesis Flow”, International Journal

of Information Science and Intelligent System (IJISIS), vol. 2, no.1, June 2013, pp. 7-25.

9 Michael Dossis, “Validation of a System Design Framework with Formal RDF Techniques: The CCC Design Framework”, International Journal of Engineering Practical Research (IJEPR), vol. 2, issue 3, August 2013, pp. 94-104.

10 Michael F. Dossis, “Use of XML Schema and Logic Programming Views as Formal Means to Validate a System Design Framework”, Open Journal of Artificial Intelligence (OJAI), vol. 1, no. 2, November 2013, pp. 18-32.

11 Michael F. Dossis, “Formal, Rapid Coprocessors from ADA Code”, News in Engineering journal, Scientific Publications (SciPub), vol. 1, issue 1, November 2013, pp. 19-28.

12 Michael F. Dossis, “Intelligent Custom Block Generation”, Universal Journal of Electrical and Electronic Engineering, Horizon Research Publishing Corporation (HRPUB), vol. 2, no. 2, February 2014, pp. 59 - 69.

13 Michael F. Dossis, and Dimitrios E. Amanatidis, “Design Automation of Neural Network Applications Using Formal Techniques—Rapid Prototyping Using the CCC Synthesizer”, International Journal of Automation and Control Engineering (IJACE), vol. 3, issue 1, February 2014, pp. 10 - 19.

14 Michael Dossis, “Synthesis of Custom Hardware from ADA with Artificial Intelligence Techniques”, Advances in Robotics and Automation, OMICS Group, ISSN: 2168-9695 ARA, an open access journal, vol. 3, no. 2, July, 2014.

15 Michael Dossis, “Custom Hardware Synthesis from UML”, International Journal of Engineering Research and Management (IJERM), vol. 1, issue 6, September 2014, pp. 173-184.

16 Michael Dossis, “High-Level Synthesis: A Practical Perspective”, Advances in Robotics and Automation, OMICS Group, ISSN: 2168-9695 ARA, an open access journal, vol. 3, no. 3, December, 2014.

17 Michael Dossis, Vasilios Hados, and Georgios Dimitriou, “Automatic Generation of Trigonometric Hardware with HLS Tools – Using the CubedC Hardware Compiler/Optimizer”, International Journal of Engineering Researches and Management Studies, vol. 1, no. 1, December 2014, pp. 15-25.

18 Michael Dossis, "Intelligent Hardware Compilation with Options: The CCC HLS system and XML schema", International Open Access Journal, Weber Engineering and Technology, vol. 1, no 1, February 2015, pp. 62-70.

19 Michael Dossis, and Dimitris E. Amanatidis, “Hardware Implementation of Geometric Active Contours”, International Journal of Engineering and Industries (IJEI), vol. 6, no. 1, March 2015, pp. 1-11.

20 Michael Dossis, and Georgios Dimitriou, “Are HLS Tools Healthy?”, Journal of Engineering, Technology & Applied Science Research, vol. 5, no. 2, April 2015, pp. 790-794.

21 Michael Dossis, “UML and HLS Methods for Audio Video Hardware”, International Journal of Intelligent Information Processing (IJIIP), vol. 5, no. 3, June 2015, pp. 21-44.

22 Nikolaos E Karkalos, Angelos P Markopoulos, and Michael F Dossis, “Application of Statistical and Soft Computing techniques for the Prediction of Grinding Performance”, Journal of Robotics and Mechanical Engineering Research, Verizona Publisher, vol. 1, no. 2, July 2015, pp. 1-11.

23 Michael Dossis, “Converging Formal Verification with High-level Synthesis”, Journal of Next Generation Information Technology (JNIT), vol. 6, no. 3, August 2015, pp. 25-36.

24 Michael F. Dossis, “High-level Synthesis Integrated Verification”, Engineering, Technology & Applied Science Research journal, vol. 5, no. 5, October 2015, pp. 865-871.

25 Amanatidis Dimitrios, Dossis Michael, Androulidakis Iosif, “Image Contour Segmentation in Hardware”, Journal of Radio Electronics, Computer Science, Control, 2015, Issue 35, no 4, pp. 66-71.

26 Michael Dossis, “Seamless Signal Processing Block Implementation Using the Cubed-C Design Environment”, International Robotics and Automation Journal, Vol. 2, Issue 4, June 21 2017.

27 Michael Dossis, and Georgios Dimitriou, “High-level Synthesis Optimizations in an Artificial Intelligence Framework”, SciFed Journal of Artificial Intelligence, Vol. 1, Issue 2, August 7, 2018.

28 Nikolaos E. Karkalos, Angelos P. Markopoulos and Michael F. Dossis, “Optimal Model Parameters of Inverse Kinematics Solution of a 3R Robotic Manipulator Using ANN Models”, International Journal of Manufacturing, Materials, and Mechanical Engineering, Volume 7, Issue 3, July-September 2017.

29 Athanasios Tziouvaras, Georgios Dimitriou, Michael Dossis, and Georgios Stamoulis, “Frequency Scaling for High Performance of Low-End Pipelined Processors”, Advances in Science, Technology and Engineering Systems Journal (ASTESJ), Volume 6, Issue 2, pp. 763-775, March 2021.

30 Dimitrios Amanatidis, Michael Dossis, “Behavioural synthesis of SGD using the CCC framework: a simple XOR-solving MLP”, Applied Intelligence, Springer, vol. 52, pp.15226–15236, 12 March 2022. Published online: https://doi.org/10.1007/s10489-022-03376-9, 11 pages, Accepted: 10 February 2022.

31 Antonios Dadaliaris, George Kranas, Panagiotis Oikonomou , George Floros and Michael Dossis, “Exploiting Net Connectivity in Legalization and Detailed Placement Scenarios”, Information 2022, MDPI, Switzerland, 13(5), 212, 20 April 2022. https://doi.org/10.3390/info13050212.

32 Amanatidis, D., Mylona, I., Dossis, M., Kamenidou, I., & Mamalis, S. (2024). Consumers’ social media engagement and online behavior: A structural equation modelling analysis. Online Journal of Communication and Media Technologies, 14(1), e202401. https://doi.org/10.30935/ojcmt/13857

33 Georgios Gkagkas; Dimitrios J. Vergados; Angelos Michalas; Michael Dossis, “The Advantage of the 5G Network for Enhancing the Internet of Things and the Evolution of the 6G Network”, MDPI Sensors 2024, Volume 24, Issue 8, 2455, Open Access Journal.

B. Chapters of international reference books and peer-review

1 Michael Dossis, "High-Level Synthesis for Embedded Systems". Chapter 16, in **Embedded System – Theory and Design Methodology**, Book 1, Edited by Kiyofumi Tanaka, InTech - Open Access Publisher, ISBN 979-953-307-580-7, March 2012, pp. 341-366.

2 Michael F. Dossis, "Formal Methods in High-Level and System Synthesis ". In the Springer Series on Studies in Computational Intelligence, edited volume entitled as **“Semantic Hyper/Multi-media Adaptation: Schemes and Applications”**, Springer-Verlag, Berlin Heidelberg, ISSN: 1860-949X, SCI 418, 2012, pp. 23-81.

3 Michael Dossis, “Formal Design Flows for Embedded IoT Hardware.” In the Springer volume edited by Georgios Keramidas, Nikolaos Voros and Michael Hubner, “**Components and Services for IoT Platforms**”, Springer International Publishing Switzerland, 2017, pp. 27-55.

4 Nikolaos E. Karkalos, Angelos P. Markopoulos and Michael F. Dossis, “Optimal Model Parameters of Inverse Kinematics Solution of a 3R Robotic Manipulator Using ANN Models”, in Book of **Deep Learning and Neural Networks: Concepts, Methodologies, Tools, and Applications**, 2020, DOI: 10.4018/978-1-7998-0414-7.ch045, January 2020.

5 Sotirios Kontogiannis, George Kokkonis, Ioannis Kazanidis, Michael Dossis, Stavros Valsamidis, “Cultural IoT Framework Focusing on Interactive and Personalized Museum Sightseeing”, in Matin M. (eds) **Towards Cognitive IoT Networks**, Springer, 26 March 2020, pp. 151-181.

C. International, periodical scientific conferences with peer-review and proceedings

1 Dossis, M. F., Noras, J. M. And Porter, G. J., "Custom Coprocessor Compilation", Proc. 3rd International Workshop On Field Programmable Logic And Applications, Jesus College, University Of Oxford, Oxford, Uk, 7-10 September, 1993. In W. Moore and W. Luk, Editors, More Fpgas, Pages 202–212. Abingdon Ee & Cs Books, 1993.

2 Dossis, M. F., Noras, J. M. And Porter, G. J., "Synthesis and Evaluation In The C Cubed System: Custom Coprocessor Compilations", Proc. 2nd International Conference On Concurrent Engineering & Electronic Design Automation, Poole, UK, 7-8 April, 1994, pp. 443-448.

3 Dossis, M. F., Noras, J. M. And Porter, G. J., "Synthesis of Customised Hardware from Ada", Proc. IEEE International Conference On Circuits And Systems, London, 30 May - 2 June, 1994, Volume 1, pp. 229-232.

4 Dossis, M. F. And Noras, J. M., "Feasibility Studies for RSA Asics Via Multilevel Simulation", The European Simulation Symposium 95, Erlangen-Nuremberg, 26-28 October 1995, pp. 416-420.

5 Dossis, M. F., "Standard Formats for Register Transfer Level VHDL Modelling", The European Simulation Symposium 95, Erlangen-Nuremberg, 26-28 October 1995, pp. 423-427.

6 Dossis, M. F., "Syntax Driven Approach for Rtl Hardware Synthesis Of Parallel Programs", IEE Colloquium On "Hardware-Software Cosynthesis For Reconfigurable Systems", Hewlett Packard Laboratories, Bristol, 22 February 1996. Iee, Computing and Control Division, Digest No: 96/036, pp. 4/1-4/16.

7 Michael Schenke and Michael Dossis: “Provably Correct Hardware Compilation Using Timing Diagrams”, In Formal Methods For Protocol Engineering And Distributed Systems: Forte Xii/Pstv Xix ‘99: IFIP Tc6 Wg6.1 Joint International Conference On Formal Description Techniques For Distributed Systems And Communication Protocols (FORTE XII) And Protocol Specification, Testing, And Verification (PSTV XIX). Edited By Jianping Wu, Samuel T. Chanson, Quiang Gao, pp. 313-331. Beijing, China, October 1999. (Forte/Pstv’99 Best Paper Award).

8 M.F. Dossis, T. Themelis, L. Markopoulos: “A Web Service To Generate Program Coprocessors”, 4th IEEE International Workshop On Semantic Media Adaptation And Personalization (IEEE SMAP ’09), San Sebastian, Spain, December 14-15, 2009, pp. 121-128.

9 Michael Dossis, “Automatic Generation of Massively-Parallel Hardware From Control-Intensive, Sequential Programs”, Proceedings Of IEEE ISVLSI 2010, Lixouri, Kefalonia, 5-7 July 2010, pp 98-103.

10 M.F. Dossis, “Using an XML Schema To Validate A Formal Hardware Compiler”, Proceedings Of 5th IEEE International Workshop On Semantic Media Adaptation And Personalization (IEEE SMAP ’10), Dec. 9-10, 2010, Limassol, Cyprus, pp. 90-97.

11 Michael F. Dossis, “Synthesis of Provaly-Correct Hardware With Options”, Proceedings Of 17th IEEE International Conference On Electronics, Circuits, And Systems (IEEE ICECS 2010), 12-15th Dec. 2010, Athens, pp. 637-640.

12 Michael F. Dossis, "Formal Generation of Synthesizable RTL From Regular Programs", Proceedings Of The 6th

IEEE Design And Technology Of Integrated Systems In Nanoscale Era, 6-8 April 2011, Athens, Greece, Paper No: 30

13 Dimitrios Amanatidis And Michael Dossis, "Use Of Behavioral Synthesis To Implement A Cellular Neural Network For Image Processing Applications", Proceedings Of The 15th Panhellenic Conference On Informatics (PCI 2011), 30 September - 2 October 2011, Kastoria, Greece, pp. 183-187.

14 Michael F. Dossis, "Using RDF And XML Techniques to Formally Validate A Hardware Design Flow", Proceedings Of The 5th International Conference From Scientific Computing To Computational Engineering, 4-7 July 2012, Athens, Greece, Volume II, pp. 483-410.

15 Michael F. Dossis, "RDF Validation of An ESL Toolset", Proceedings Of The 1st Virtual International Conference On Advanced Research In Scientific Areas (ARSA-2012) Slovakia, December 3-7, 2012.

16 Michael F. Dossis, "Rapid Coprocessors from Ada Code; Using The CCC Synthesizer", Proceedings Of The 1st Global Virtual Conference, April 8-12 2013, pp. 489-494.

17 Michael F. Dossis, "Mapping Custom Blocks in High-Level Synthesis", Proceedings Of The 5th International Conference On Experiments/Process/System Modeling/Simulation/Optimization (5th Ic-Epsmso), Athens, 3-6 July, 2013, pp. 314-321.

18 Michael Dossis, "Custom Options for Custom Processors", Proceedings Of The 1st International Virtual Scientific Conference, Zilina, Slovakia, June 10-14, 2013, pp. 370-375.

19 Michael Dossis, "Modeling and Simulation In A Formal Design Framework", Acm Proceedings Of The 6th Balkan Conference In Informatics, Thessaloniki, Greece, September 19-21, 2013, pp. 31-38.

20 Michael Dossis, And Kostas Koufakis, "Combining Floating-Point Designs In High-Level Synthesis", In Proceedings Of The 2nd Conference Of Advanced Research In Scientific Areas (2nd Arsa 2013), December, 2-6, 2013, Slovak Republic, pp. 382-386.

21 Michael Dossis, "Custom Hardware Arithmetic Via High-Level Synthesis", In Proceedings Of The WOCSDICE 2014 Conference, 15-18 June, 2014, Delphi, Greece, pp. 117-118.

22 Michael F. Dossis, "Hardware Synthesis of IEEE FP Arithmetic From Ada", In Proceedings Of The 6th Ic-SCCE Conference, 9 – 12 July, 2014, Athens, Greece, pp. 210-217.

23 Michael Dossis, "Automatic Compilation of FP Hardware", In Proceedings Of The 2nd International Virtual Scientific Conference (Scieconf), Slovakia, June 9-13, 2014, pp. 418-422.

24 Michael Dossis, "Practical Aspects of HLS Tools", In Proceedings Of The 3rd Electronic International Interdisciplinary Conference, September 1-5, 2014, pp. 419-422.

25 Michael F. Dossis, "A Floating-Point Paradigm For High-Level Synthesis", In Proceedings Of The 18th Panhellenic Conference On Informatics (Pci 2014), 2-4 October 2014, Harokopion University, Athens, Greece, 6 Pages.

26 Michael Dossis, "Audio-Video Coprocessor Synthesis From UML", In Proceedings Of The Research Conference In Technical Disciplines Rcitd 2014, November 17-21, 2014, pp. 12-17.

27 Michael Dossis, And Vasilios Hados, "High-Level Synthesis In Trigonometric Applications", In Proceedings Of The Advanced Research In Scientific Areas Conference, 1-5 December, 2014, pp. 286-292.

28 Michael Dossis, Vasilios Hados, And Georgios Dimitriou, “Numerical Block High-Level Synthesis”, In Proceedings Of The International Conference On Computer Science, Computer Engineering, And Social Media, Thessaloniki, Greece, December 12-14, 2014, pp. 29-40.

29 Michael Dossis, Vasilios Hados, And Georgios Dimitriou, “Hardware Trigonometry With High-Level Synthesis”, In Proceedings Of The Virtual Multidisciplinary Conference QUAESTI 2014, December 15-19, 2014, pp. 495-500.

30 Michael Dossis, “HLS and Practical Issues”, In Proceedings Of The Panhellenic Conference In Electronics And Telecommunications PACET 2015, Paper 56, Ioannina 8-9 May, 2015.

31 Dimitrios Amanatidis, Michael Dossis, And Iosif Androulidakis, “Hardware Representation Of A Contour-Based Image Segmentation Method”, In Proceedings Of The Panhellenic Conference In Electronics And Telecommunications PACET 2015, Paper 57, Ioannina 8-9 May, 2015.

32 Georgios Dimitriou, And Michael Dossis, “Experimenting With A High-Level Synthesis System Front End”, In Proceedings Of The Panhellenic Conference In Electronics And Telecommunications Pacet 2015, Paper 66, Ioannina 8-9 May, 2015.

33 Michael Dossis, “Designing Digital Hardware Using UML And Behavioural Synthesis”, In Proceedings Of The 3rd Global Virtual Conference Gv-Conf 2015, Thomson, Slovakia, 6-10 April, 2015, pp. 135-142.

34 Michael Dossis, “High-Level Synthesis In Practice”, In Proceedings Of The 4th International Virtual Scientific Conference On Informatics And Management Sciences (Ictic 2015), 23-27 March, 2015, Www.Ictic.Sk, pp. 70-74.

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49 Michael Dossis, And Georgios Dimitriou, “High-Level Optimizations For High-Level Synthesis”, In Proceedings Of ISERD International Conference, Athens, Greece, 7th-8th December 2017, pp. 6-13.

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Timing Analysis in Pipelined Processors", In proceedings of the 4th IEEE South-East Europe Design Automation, Computer Engineering, Computer Networks, And Social Media Conference (SEEDA_CECNSM 2019), September 20-22, 2019, University of Piraeus, Piraeus, Greece, https://seeda2019.unipi.gr/, pp. 15-20.

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6.3 Research & Development technical reports:

1 Dossis, M. F. and Noras, J. M., "A Compiler System for use in E-CAD", Technical report, University of Bradford, dep. of Electronic and Electrical Engineering, October 1994, Report no: 556.

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3 Dossis, M. F. and Noras, J. M., "Portable Ada coding of embedded coprocessors", Technical report, University of Bradford, dep. of Electronic and Electrical Engineering, February 1995, Report no: 563.

4 Dossis, M. F. and Noras, J. M., "Standard formats for Register Transfer Level modelling in VHDL", Technical report, University of Bradford, dep. of Electronic and Electrical Engineering, February 1995, Report no: 564.

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8 Dossis, M. F. and Noras, J. M., "Optimising and verifying hardware algorithms for RSA public-key cryptography", Technical report, University of Bradford, dep. of Electronic and Electrical Engineering, February 1995, Report no: 569.

9 "Multicarrier Demodulator with Frequency-Domain Symbol Timing Correction", contribution to the European Space Agency Contract Report No: 539, May 1994.

7. Citations of (references to) my research publications (international recognition of my contributinons):

1. Koen Claessen: "Embedded Languages for Describing and Verifying Hardware", Thesis for the Degree of Doctor of Philosophy, Department of Computing Science, Chalmers University of Technology and Goteborg University, Goteborg, Sweden, April 2001.
http://www.cs.chalmers.se/pub/users/koen/Papers/phd.ps

2. Koen Claessen and Gordon Pace, "An Embedded Language Framework for Hardware Compilation", Conference on Correct Hardware Design and Verification Methods (CHARME), 2000.
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4. Scott Hauck and Anant Agarwal: "Software Technologies for Reconfigurable Systems", Northwestern University, Dept. of ECE, Technical Report, 1996. Submitted to IEEE Transactions on Computers. Northwestern University, Department of ECE, Dept. of ECE.

http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.36.7849&rep=rep1&type=pdf and http://www.ecs.umass.edu/ece/tessier/courses/697c/hauck-system.pdf

5. Goran Doncev, Miriam Leeser and Shantanu Tarafdar: "Truly Rapid Prototyping Requires High Level Synthesis". In proceedings of the 9th International Workshop on Rapid System Prototyping, 3-5 June 1998, Leuven , Belgium, pp. 101-106. http://ieeexplore.ieee.org/iel4/5571/14905/00676676.pdf

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10. Jorg Bottger, Wolfgang Ecker “Comparing Ada'95 and VHDL for Behavioral Hardware Description on Causal and Synchronous Level”. In Proc. of VHDL user's forum in Europe : SIG-VHDL Spring'97 working conference, 1997, Toledo, Spain, pp. 147-158. (it references my paper: “Synthesis of Customized hardware from ADA”)

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12. David Stevens, et. al., “BioThreads: A Novel VLIW-Based Chip Multiprocessor for Accelerating Biomedical Image Processing Applications”, IEEE Transactions on Biomedical Circuits and Systems, June 2012, vol. 6, issue 3, pp: 257-268. (it references my paper: “A web service to generate program coprocessors”)

13. Nader Fakhry, Viswanathan Lakshmanam, “Verilog to Vital Translator”, US Patent 6668359 B1, December 23, 2003. (it references my paper: "Synthesis Of Customised Hardware From Ada"). Can be also accessed from: http://www.patentstorm.us/patents/6668359.html

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17. S Guillet, F Lamotte, N Griguer, É Rutte, et al. “Extending UML/MARTE to Support Discrete Controller Synthesis, Application to Reconfigurable Systems-on-Chip Modeling”. ACM Transactions on Reconfigurable Technology and Systems (TRETS) - Special Issue on 11th International Conference on Field-Programmable

Technology (FPT'12) and Special Issue on the 7th International Workshop on Reconfigurable Communication-Centric Systems-on-Chip (ReCoSoC'12), Volume 7 Issue 3, August 2014, Article No. 27.

18. K Sano, H Suzuki, R Ito, T Ueno, et al. “Stream Processor Generator for HPC to Embedded Applications on FPGA-based System Platform”. Presented at First International Workshop on FPGAs for Software Programmers (FSP 2014).

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21. J. Bottger, and W. Ecker, “Comparing Ada'95 and VHDL for Behavioral Hardware Description on Causal and Synchronous Level”, VHDL User's Forum in Europe: SIG-VHDL Spring'97 Working Conference, 1997.

22. L. Zhu, and Z. Fang, “Modeling and simulation of mixed-signal integrated circuits based on Verilog-AMS”, 2nd International Symposium on Instrumentation and Measurement, Sensor Network and Automation (IMSNA), 2013, pp. 1–4.

23. Jianliang Guo, Jun Chi and Lianqing Chen, “Estimation of Grinding Force with Consideration of Rupture Factor”, IOP Conf. Series: Materials Science and Engineering 470 (2019) 012027, IOP Publishing, doi:10.1088/1757-899X/470/1/012027, ICMEAS 2018, 9 pages.

8. International Patents:

1. At 5/10/06 the Greek Industrial Property Organisation, awarded to Michael Dossis the international patent 1005308 titled: “**Method of Translating Programs into Hardware Description**”.

2. At 4/7/2008 the Greek Industrial Property Organisation, awarded to Michael Dossis the international patent 1005968 titled: “**Generalised communication method between application-specific co-processor circuits**”.

3. At 15/4/2009 the Greek Industrial Property Organisation, awarded to Michael Dossis the international patent 1006354 titled: “**Intermediate Tables Format for use in Program Compilers and Design Tools**”.

4. At 25/11/2009 the Greek Industrial Property Organisation, awarded to Michael Dossis the international patent 1006609 titled: “**Method of Accelerating Programs with Decision Triangles**”.

5. At 1/12/2009 the Greek Industrial Property Organisation, awarded to Michael Dossis the international patent 1006614 titled: “**Method of Optimizing Digital Circuits with Hierarchical Karnaugh Maps**”.

9. Supervision of graduation and final year projects:

1995: "Analysis and visualisation of design flow-graphs with GUI and object-oriented programming techniques", BEeng final year project, dept of Electronic and Electrical Engineering, University of Bradford, UK.

2009-2010: “Implementation of algorithms for DSP in hardware, using advanced design tools”, Final-Year Project, department of Informatics and Computer Technology, Technological Educational Institute of Western Macedonia.

2010-2011: "Graphical visualization of the Intermediate Tables Format", Final-Year Project, department of Informatics and Computer Technology, Technological Educational Institute of Western Macedonia.

2011-today: A large number of final year projects in the department of Informatics Engineering, TEI of Western Macedonia.

10. Lab, research & teaching experience related to digital circuit & system design:

- Device Modelling in Pspice, Elec. Eng., BEeng 2nd year, 60 hours, 1991.
- Project Labs in Telecommunications (ASIC design), Elec. Eng., BEeng 2nd year, 17 hours, 1991.
- Design Project (ASIC), Elec. Eng., BEeng 2nd year, 66 hours, 1992.
- Enterprise Project (microprocessor-based control system), Elec. Eng., BEeng 2nd year, 90 hours, 1992.
- Tutorial & Lab in Digital Processes 2 (FSM design, 68000 real-time design/assembler), Elec. Eng., BEeng 2nd year, 54 hours, 1992.
- Tutorial & Lab in Digital Processes 3 + Devices & Device Modelling Tutorial (Electronic Physics + SPICE modelling), Elec. Eng., BEeng 2nd year, 60 hours, 1993.
- Design Project (microprocessor-based control), Elec. Eng., BEeng 2nd year, 36 hours, 1993.
- Structured Assembler (Motorola MC680xx), Elec. Eng., MEeng real-time systems, BEeng 18 hours, 1993.
- Digital Processes 3 (FSM design + 68000 architecture), Elec. Eng. 2nd year, BEeng 60 hours, 1994.
- Design Project (microprocessor-based control), Elec. Eng., 2nd year, BEeng 24 hours, 1994.
- Senior Teaching Assistant with the PACE Teaching Company Scheme, 1/5/94 - 30/11/94.
- Part-time lecturer in the following: Computer Graphics with (Borland) C++, Elec. Eng., EIMC Research Unit (Electronic Imaging and Multimedia Computing), BSc 2nd year, 16 hours, 1994.
- Lecturer: "(DSP) Processor Architectures" (DSP theory and design with TMS32xxxx), Elec. Eng., BEeng 3rd year + MEeng, 40 hours, 1994-1995.
- Lecturer-supervisor: "Analysis and visualisation of design flow-graphs with GUI and object-oriented programming techniques", BEeng final year project, 1995.
- Demonstrator and design specialist consultant: ASIC design course & lab, Oxford University, dep. of Engineering Science, BSc final year, 27 hours, April & May 1996.
- Digital Design with Xilinx Spartan FPGAs and Xilinx ISE Design Suite and EDK, TEI of Western Macedonia, since 2007.
- TRN (training computer model) emulator in computer architecture labs, TEI of Western Macedonia, since 2007.
- Collaborating with world-leading research group on EDA tools and use of OpenCL to deliver FGPA accelerators (Volos, Greece), 2011-2012.
- Collaborative research with Digital Design and computer arithmetic for High-level Synthesis research group of NTUA, Athens, Greece, 2012.

11. Academic administrative positions and member in academic committees

- Πresident of the departments of Informatics of the University of Western Macedonia
- Deputy president of the departments of Informatics and Computer Technology and Informatics Engineering of the TEI of Western Macedonia
- President of the security committee of the Kastoria Campus of the TEI of Western Macedonia
- President of the replacement spare parts of the Kastoria Campus of the TEI of Western Macedonia
- Member of the committee for evaluation of the applications for teaching/scientific associates of the departments of Informatics and Computer Technology and Informatics Engineering of the TEI of Western Macedonia
- Member of the committee of the weekly teaching schedule of the departments of Informatics and Computer Technology and Informatics Engineering of the TEI of Western Macedonia
- Member of the committee of industrial placement of the departments of Informatics and Computer Technology and Informatics Engineering of the TEI of Western Macedonia
- Member of the evaluation committee for the new premises of the Kastoria campus of the TEI of Western Macedonia

- Member of the committee of admission exams for joining the department of Informatics Engineering
- Adoption of USA-made electronic equipment and E-CAD software for the Digital Design Labs of the departments of Informatics and Computer Technology and Informatics Engineering of the TEI of Western Macedonia
- President of the heating fuel committee of the Kastoria campus of the TEI of Western Macedonia
- Member of the committee for advancing and certification of the studies curriculum of the department of Informatics Engineering of the TEI of Western Macedonia
- Elector for a number of members of staff of academic positions in Greece

12. Attendance of seminars and development/training courses

- "ASIC VLSI design with SOLO 1400", European Silicon Structures Ltd, NTUA, Athens, March 1990.
- "Orientation to University Teaching Programme", Management Centre, Teaching & Learning Development Unit, University of Bradford, 19 to 21 September 1994.
- "Handling Information Overload", Management Centre, Teaching & Learning Development Unit, University of Bradford, 5 to 6 January 1995.
- "Consultancy Skills", University of Bradford, TLDU, Six Flags Hotel, 10 April 1995.
- "Rapid Reading", University of Oxford, Staff Development Office, University Offices, Wellington Square, & Dep. of Continuing Education, Oxford, 13 November 1995.
- "Writing Research Papers, Abstracts and Posters", University of Oxford, Staff Development Office, University Offices, Wellington Square, Oxford, 16 November 1995.
- "Project Management", using Microsoft Project for Windows. John Munday & associates, LSI Logic Europe premises, 6 to 8 January 1997, UK
- "How to Design and Implement Digital Wireless Communications Systems", a Digital Wireless Seminar by Ravi Subramanian of Synopsys. Hewlett Packard premises, 24 February 1997.
- "Synopsys Chip Synthesis Course", Synopsys. 4-day advanced modelling, synthesis, implementation and & chip design course, Synopsys premises, 7 to 10 October, 1997.
- "Synopsys Spring Seminar", Synopsys, Synthesis tools and design flows, Virginia Water, Berks, 8 May, 1998.
- "Static Timing Analysis with PrimeTime", Synopsys. Intracom SA premises, Paiania, Attiki, 2 to 6 August 2004.
- "One day workshop on Synopsys chip design tools", Synopsys. Corallia Site, Marousi, Athens, 10 July 2008.
- Training Seminar on "Grid Technology", National Centre for Research & Technology, (ΕΔΕΤ), TEI of West Macedonia, Kastoria, 12-13 of March, 2009.
- "Training seminar on Cadence design tools, inc. front-end, RTL-low power synthesis, formal verification, mixed-signal design, sign-off, and back-end flow", Cadence. Corallia Site, Marousi, Athens, 1 July 2009.

13. Technical Affiliations:

- Special Session Chair, in SEEDA_CECNSM 2021, (C1: Computer Engineering and Design Automation), University of Ioannina, Preveza, Greece
- Special Session Chair, in SEEDA_CECNSM 2021, 3 Special Sessions, University of Ionian Isles, Virtual Conference
- General Co-Chair at SEEDA_CECNSM 2019, 2020, 2021 international conference.
- General Chair at SEEDA_CECNSM 2016, 2017, 2018 international conference, Kastoria, September 2016, 2017, 2018.
- Member of organizing committees of conferences: SEEDA_CECNSM, PCI, PACET, RCITD.
- Special Session Chair (High-level Synthesis, CAD and Applications) at Panhellenic Conference in Electronics and Telecommunications PACET 2015, and Social Media, Ioannina, 8-9 May, 2015
- Special Session Chair (High-level Synthesis, CAD and Applications) at International Conference on Computer Science, Computer Engineering, and Social Media, Thessaloniki, Greece, December 2014.
- Reviewer for the British Journal of Mathematics and Computer Science

- Member of the Program Committee for the FPL 2014 conference
- Editor of the International Journal of Automation and Control Engineering (IJACE), Science and Engineering Publishing Company, http://www.seipub.org/ijace/ -> Editorial Board
- Editor-in-Chief of the Journal of Software Engineering, Bioinfo Publications
- Associate Editor-in-Chief of the scientific Journal of Next Generation Information Technology (JNIT)
- Editor of the scientific International Journal of Intelligent Information Processing (IJIIP)
- Editor of the scientific International Journal of Advancements in Computing Technology (IJACT)
- Editor of the scientific International Journal of Engineering and Industries (IJEI).
- Member of: Computer Simulation Society, VHDL, DASC, SCL, EDIF & other working groups.
- Member of the Technical Chamber of Greece since 1990.
- Member of the Technical Chamber of Greece Expert Scientific Committee on Electronic Systems.
- Member of the organizing committee and technical support manager for the International Conference Of Applied Economics (ICOAE 2008/2009), Kastoria, May 2008 and May 2009.
- External reviewer/evaluator of research papers, for the «*Advances in Science, Technology and Engineering Systems Journal*»
- External reviewer/evaluator of research papers, for the IEEE/ACM Design Automation Conference.
- Reviewer/evaluator of research papers, for the IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2010.
- Reviewer/evaluator of research papers, for the IEEE 11th International Conference on Industrial Informatics, Bochum, Germany, July 29-31, 2013.
- Reviewer of research papers, for the International Journal of Engineering Practical Research (IJEPR).
- Reviewer of research papers in the International Journal: ACM Transactions on Reconfigurable Technology and Systems.
- Reviewer/evaluator of research proposals in the programme Collaboration ("Synergasia") of the General Secretariat of Research and Technology (GGET) (2010).

14. European-funded research projects:

- OMI/HORN - 7249 – "Highly Optimised Reusable Nucleus". ESPRIT project, at University of Oxford. (for more details look in: http://web.comlab.ox.ac.uk/oucl/research/grants/lr.html)
- IST – ADRIATIC, Intracom Telecom 2000
- Hermes Project, Technical University of Krete, 2013
- European programme: **Universal WiFi Platform**, In collaboration with the University of Patras. Design, development and verification in FPGAs of Channel Estimation System in VHDL for the IEEE 802.11p standard.

15. Other interests/hobbies/activities

- Classical and jazz music. Composition and improvisation
- Cycling, jogging, travelling, target shooting, sea sports
- In charge of the Technical Department and member of Organising Committee of International Conference of Applied Economics, Kastoria, May 2008 and May 2009 (ICOAE 2008/2009).

B. Expertise in – technical skills developed:

- Digital design; synchronous design principles & guidelines, synchronous sequential machines, Boolean algebra, Karnaugh maps - Veitch diagrams for min-term optimisation
- Synopsys HDL (VHDL/Verilog) compiler, Design Compiler
- Synplicity Synplify/Amplify synthesis tools
- VHDL/Verilog for simulation and synthesis.
- Simulators: MODELSIM, VCS

- ECAD technology; Tools, design entry, design flow, libraries, silicon compilers, test vector generation waveform facilities, behavioural, RTL, logic, gate-level circuit description, netlists, EDIF interfacing.
- High-level behavioural, RTL and logic synthesis
- CADENCE Verilog composer (synthesis tool).
- CADENCE VHDL-XL libraries and simulation with waves.
- CADENCE Synergy VHDL Synthesizer & Optimiser, and its modelling style (v. 1.3).
- European Space Agency, VHDL modelling guidelines.
- TTL 74xxx base libraries (primitive elements, counters, adders, BCD encoders, etc.)
- Low-level digital NMOS/CMOS transistor design: CMOS gates, muxes, combinatorial blocks, pass-transistors, buffer design, Domino Logic, transmission gates, cascade logic, bit-serial design, capacitance/delay issues, p-well & n-well process, I/O, tri-state and bidirectional pads, clocking and clock-buffering fanout strategies (fanout buffer trees, etc.), Built-in Self Test design approaches, fast computer arithmetic with CMOS (adders, multipliers, carry lookahead, carry save, redundant modulo-4 and modulo N^2 arithmetic implementations.
- ES2 libraries (2, 1.5, 1.2 technologies), SOLO 1400 MODEL silicon compiler, DRAFT schematic entry tool waveform simulation capability, SHIP-DES, and PACKAGE multiplier/ROM/RAM megacell generator compiler.
- Design of Moore & Meally Finite State Machines, using booth state diagrams & synthesis facilities (VHDL/Verilog).
- Viewlogic, Powerview (ViewSynthesis) VHDL modelling style & guidelines.
- Simulation and Test Language (STL simulation) with CADENCE
- ABEL hardware synthesis language for PLDs
- Mietec, Standard Cell, 2.4 um design libraries with CADENCE, their Verilog libraries and for full custom design.
- Altera, Xilinx FPGAs
- Max+Plus 2, XACT design and Place & Route tools
- General-purpose microprocessor architecture: Intel 286/386, Motorola (68xxx)
- Custom processor architectures; DSP (Texas Instr., Harvard Architecture); DSP filters (convolvers, FIR filters) Fast Fourier Transform hardware architectures.
- ALUs & datapaths, Controller design, Bus design, Scratch-pad registers, latches, RAMs, Buffers and FIFOs, encoding/decoding, fast arithmetic and IEEE Floating-Point hardware arithmetic design.
- Digital communications (protocols, routers, switchers, Broadband/ISDN design)
- Asynchronous I/O & communication protocol design techniques
- Design for cryptography & data security (encryption & RSA)
- Programming with Ada, PASCAL, C, C++, Prolog, Occam, SML, HTML
- Computer architecture, interrupts, operating systems, Assembly, I/O and peripherals, data structures, data-base design
- Microprocessor based & digital control
- Design for parallel architectures (transputer based, massively parallel machines, pipeline, multi datapath and pipelined controller (finite state machine) design
- Functional, netlist and annotated netlist verification in VHDL and Verilog.
- test methodologies, module verification, mixed mode simulation, test coverage, fault test, test pattern generation and re-targeting.
- applied formal methods, model checking, FSM verification
- OpenCL for software and hardware implementations
- Matlab language programming and use of the Matlab DSP toolbox